In the Claims

Please amend the claims as indicated below. This listing of claims replaces all prior versions.

1. (currently amended) A bus system comprising a first and second station ~~(10, 14)~~ coupled via a bus ~~(12)~~ for transferring data and control signals, the bus ~~(12)~~ operating according to a protocol in which the first station ~~(10)~~ repeatedly sends requests ~~(200, 210, 220, 230)~~ for data to the second station, the second station ~~(14)~~ responding to each request ~~(200, 210, 220, 230)~~ by sending a message with a data item or sending a negative acknowledge signal ~~(24)~~, wherein the second station ~~(14)~~ comprises:

[[-]] an interruptable processor ~~(15)~~ for generating data items;

[[-]] a first in first out buffer ~~(160)~~ coupled between the processor ~~(15)~~ and the bus ~~(12)~~, for buffering data items for successive messages in a first in first out order, the processor ~~(15)~~ being programmed to start writing the data items to the buffer ~~(160)~~ in response to an interrupt ~~(204, 234)~~;

[[-]] a bus interface ~~(162)~~ arranged to handle the protocol, sending data items from the buffer ~~(160)~~ in the messages, the bus interface ~~(162)~~ sending an interrupt to the processor ~~(15)~~ in response to selected ones of the requests ~~(200, 210, 220, 230)~~, when the buffer is empty and no interrupts have yet been generated since the processor has written into the buffer.

2. (original) A bus system according to Claim 1, wherein the bus system is a USB bus system.

3. (currently amended) [[An]]A bus system according to claim 1, wherein the bus interface ~~(160)~~ is arranged generate an interrupt signal in response to an acknowledge signal from the first station ~~(10)~~ after sending the message.

4. (currently amended) A bus interface integrated circuit, comprising:

[[-]] a connection for a bus ~~(12)~~;

[[-]] a first in first out buffer ~~(160)~~;

[[-]] an interrupt output ~~(164)~~ for applying an interrupt to a processor ~~(15)~~;

[[-]] a controller ~~(162)~~ arranged to receive requests ~~(200, 210, 220, 230)~~ for data from the connection ~~(12)~~, and to respond to the requests ~~(200, 210, 220, 230)~~ by sending a message containing a data item from the buffer ~~(160)~~ if the buffer ~~(160)~~ is not empty, or by sending a negative acknowledge signal to the connection if the buffer is empty and to send an interrupt signal to the interrupt out put ~~(164)~~ when the buffer is empty on receiving one of the requests~~(200, 210, 220, 230)~~, but only if no interrupt ahs yet been sent since data has been written into the buffer ~~(160)~~.

5. (currently amended) An integrated circuit according to claim 4, arranged to generate an interrupt signal in response to an acknowledge signal from the bus after sending the message.

6. (currently amended) An integrated circuit according to claim 4, arranged to be switchable between a plurality of modes of operation, the integrated circuit generating the interrupt signal to the interrupt output when the buffer is empty on receiving one of the requests, but only if no interrupt has yet been sent since data has been written into the buffer in a first one of the modes, the integrated circuit generating an interrupt signal in response to an acknowledge signal from the[[_]] bus after sending the message in a second one of the modes.

7. (currently amended) An integrated circuit according to claim 4, arranged to be switchable between a plurality of modes of operation, the integrated circuit generating said interrupt signal in response to each request for data when the buffer is empty in a first one of the modes, the integrated circuit generating the interrupt signal to the interrupt output when the buffer is empty on receiving one of the requests, but only if no interrupt has yet been sent since data has been written into the buffer in a second one of the modes.

8. (currently amended) A station for connection to a bus, the station comprising:

[[-]] a connection for a bus ~~(12)~~;

[[-]] a processor ~~(15)~~;

[[-]] a first in first out buffer ~~(160)~~;

[[-]] an interrupt output ~~(164)~~ coupled to the processor ~~(15)~~;

[[-]] a controller ~~(162)~~ arranged to receive requests ~~(200, 210, 220, 230)~~ for data from the connection ~~(12)~~, and to respond to the requests ~~(200, 210, 220, 230)~~by sending a message containing a data item from the buffer ~~(160)~~ if the buffer ~~(160)~~ is not empty, or by sending a negative acknowledge signal to the connection if the buffer ~~(160)~~ is empty and to send an interrupt signal to the interrupt output ~~(164)~~ when the buffer ~~(160)~~ is empty on receiving one of the requests~~(200, 210, 220, 230)~~, but only if no interrupt has yet been sent since data has been written into the buffer ~~(160)~~.

9. (original) A station for connection to a bus according to Claim 8, arranged to operate as a USB station.